NSF/Intel Partnership on Foundational Microarchitecture Research (FoMR)

NSF/Intel Partnership on Foundational Microarchitecture Research (FoMR)

Tao Li (NSF), Yan Solihin (NSF)
Matt Haycock (Intel), Jeff Parkhurst (Intel), Hong Wang (Intel)

November 7, 2017

Agenda

- Overview
- Solicitation highlights
- Points to remember
- Questions and answers

The FoMR Program

- The NSF/Intel Partnership on Foundational Microarchitecture Research will support transformative microarchitecture research targeting improvements in instructions per cycle (IPC).

- This solicitation seeks microarchitecture technique innovations beyond simplistic, incremental scaling of existing microarchitectural structures.

The FoMR Program

- FoMR is seeking the following characteristics
  - Techniques targeting high Instructions per Cycle (IPC)
  - Microarchitecture ``turbo”: marshalling chip resources and system bandwidth to boost single thread performance
  - Efficient code generation targeting IPC

Example Areas of Interest (not exhaustive)

- Microarchitecture and code generation to boost branch prediction accuracy
- Instruction scheduling and organization of execution resources for very large instruction window processors
- Next-generation prefetchers
- Cache management
- Machine learning and data analytics-based approach
- Utilization of new microarchitecture building blocks
- Microarchitecture support for efficient compiler code generation
- Criticality-oriented design and techniques
- Microprocessor and process co-optimization

FY18 Solicitation (NSF 17-597)

https://www.nsf.gov/pubs/2017/nsf17597/nsf17597.htm

- Proposal
  - Up to $500k
  - Up to 3 years
- Estimated 6 awards
- Proposals are due January 12, 2018.

Eligibility Information

- Who May Submit a Proposal?
  - Academic Institution (universities or 2- or 4-year colleges in the US) on behalf of their faculty
- Who May Serve as PI?
  - There are no restrictions or limits on who may serve as PI
- Limit on Number of Proposals per PI or co-PI?
  - May participate as PI, co-PI, or senior personnel in no more than one proposals in this competition

Required Supplementary Documentation

- List of project personnel
  - Lead institution provides this
- Collaboration plan (limited to 2 pages)
  - If at least 2 investigators
- Data management plan (limited to 2 pages)
- Description of mentoring activities for postdoctoral researchers, if requesting funding to support any (limited to 1 page)

Collaboration Plan

- Required for each proposal if there are at least two investigators
  - Distinct expertise provided by the PIs

- Up to 2 pages

- **Proposals with at least two investigators but without this document will be returned without review**

Questions and Answers

- Q: How can I tell whether my proposed research is a good fit for the FoMR program?

- A: We are seeking the following characteristics
  - Techniques targeting high Instructions per Cycle (IPC)
  - Microarchitecture ``turbo”: marshalling chip resources and system bandwidth to boost single thread performance
  - Efficient code generation targeting IPC

Questions and Answers

- Q: Should I discuss my proposal with NSF Program Directors?

- A: Yes, PIs are encouraged to discuss planned proposals with Program Directors to assist them in determining whether FoMR is a suitable program for the work. Please be considerate of Program Directors' time and refrain from scheduling separate meetings or calls with multiple Program Directors in the same program. Once submitted, the substance of proposals will not be discussed by NSF Program Directors, as this would constitute unfair competition, or the perception thereof.

Questions and Answers

- Q: Do FoMR proposals count against the Directorate for Computer & Information Science & Engineering (CISE) Core program limits on number of proposals allowable per year?

- A: No. The limits imposed by the CISE Core programs do not apply. No person, however, can be PI, co-PI, or senior personnel on more than one FoMR proposal.

For more information:

- Slides and script available at: http://www.nsf.gov/events/
- NSF Program Director contacts:
  - taoli@nsf.govTao Li, Computing and Communication Foundations (CCF)
  - ysolihin@nsf.gov Yan Solihin, Computer and Network Systems (CNS)
- Intel contacts:
  - matthew.haycock@intel.com Matt Haycock, Center Executive Sponsor, Vice President, Intel Labs
  - jeff.parkhurst@intel.com Jeff Parkhurst, Center Program Director, Intel Labs
  - hong.wang@intel.com Hong Wang, Center Managing Sponsor, Intel Fellow, Intel Labs