



# **Real-Time Machine Learning** **(RTML)**

**Information Webcast**  
**April 3, 2019**

**NSF-RTML Solicitation: NSF 19-566**



# AGENDA

**3:00 p.m. Welcome and Introduction**

- ❖ Rance Cleaveland, Division Director, CISE/CCF
- ❖ Filbert Bartoli, Division Director, ENG/ECCS

**RTML Team Members:**

- ❖ Sankar Basu, Program Director, CISE/CCF
- ❖ Jenshan Lin, Program Director, ENG/ECCS

**3:10 p.m. Overview of NSF-RTML Program Solicitation**

**3:45 p.m. Questions & Answers**

**4:00 (or earlier) Adjourn**



# **‘Housekeeping Notes’**

## **AFTER THE MEETING**

- ❑ **After the meeting, a video recording of this webcast as well as a copy of the slides will be archived and available from the CISE website:**

[https://www.nsf.gov/events/event\\_summ.jsp?cntn\\_id=298083&org=CISE](https://www.nsf.gov/events/event_summ.jsp?cntn_id=298083&org=CISE)

- ❑ **Questions will be taken at the end of this Webinar**
- ❑ **After the meeting, you can submit questions to:**
  - **Email: [sabasu@nsf.gov](mailto:sabasu@nsf.gov), [jenlin@nsf.gov](mailto:jenlin@nsf.gov)**



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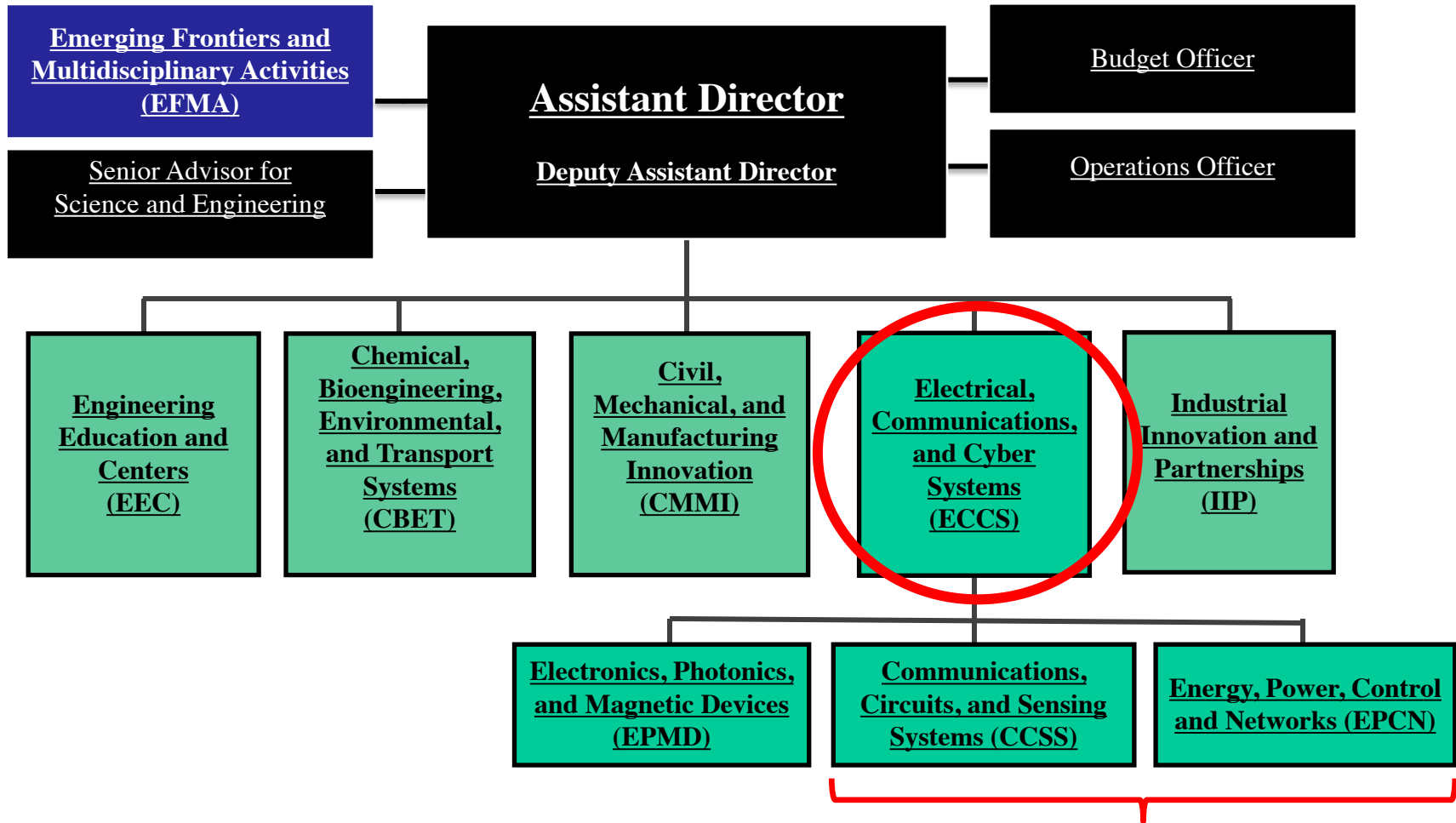
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# Purpose of Webcast

**The purpose of this webcast is:**

- ❑ To inform the community about the NSF-RTML Program Solicitation.**
- ❑ Describe collaboration with the DARPA-RTML broad agency announcement.**
- ❑ To respond to questions from potential applicants.**



# Programmatic GOALS

- ❑ NSF and DARPA will explore rapid development of energy efficient hardware architectures for ML from continuous stream of real time data, considering distributed ML in a cloud environment.
- ❑ Target application areas for DARPA
  - High bandwidth image processing in SWaP constrained systems
  - High bandwidth wireless systems such as 60 GHz 5G
- ❑ NSF-RTML program is dedicated to path-finding research in this context.
- ❑ DARPA-RTML program will create the tools and circuit development infrastructure enabling *rapid* innovation in resulting ML hardware.
- ❑ Collaboration will be effected through “**partnership supplements**” and four (4) **joint workshops** mandatory for the awardees during Phase-I and II of the DARPA project.



# DARPA Collaboration

- ❑ NSF-RTML and DARPA-RTML are two **distinct** programs.
- ❑ Solicitation, proposals submission, review criteria are different, and follow guidelines of the respective agencies.
- ❑ Funding will not be co-mingled, i.e., no cofunding will be provided by DARPA for NSF projects, or by NSF for DARPA projects.
- ❑ The two programs have **closely related** technical goals, and may provide opportunities for collaborations between the awardees through "***partnership supplements***".
- ❑ NSF encourages, but will not require, the two DARPA target applications.





# Technical goals

- ❑ DARPA Phase I will produce a *silicon compiler* benchmarked using *standard* ML frameworks.
  - At the end of Phase I, DARPA silicon compiler will be available to NSF awardees for (optional) evaluation of their algorithms.
  - Results of NSF awards will be available to DARPA teams for implementation Phase 2.
- ❑ NSF: hardware implementation in platforms integrable into silicon (FPGA or ASIC).
- ❑ DARPA: (ASICs) 14nm Silicon CMOS technologies.
- ❑ Metrics: size, weight, power, latency, and platform adaptability.



# NSF-RTML Topics

*Standard ML techniques include (but not limited to):*

- Feed forward (**convolutional**) neural networks;
- **Recurrent** networks and specialized versions (e.g., liquid-state machines);
- Neuroscience-inspired architectures, such as **spike time-dependent** neural nets including their stochastic counterparts;
- Non-neural ML architectures inspired by **psychophysics** and derived from **classical statistical mechanics**;
- Classical **supervised learning** (e.g., regression and decision trees); **unsupervised learning** (e.g., clustering), **Semi-supervised** learning methods;
- **Generative Adversarial Networks** (GAN) techniques;
- Other approaches, e.g., transfer learning, reinforcement learning, manifold learning and one-shot learning, including lifelong learning algorithms.
- *Routine implementations of known ML algorithms in existing hardware are not within scope.*



# More technical guidelines ...

- ❑ Hardware-software-algorithm cross-layer **co-design** is required;
- ❑ Learning algorithms in which **all stages of training** (including incremental training, hyperparameter estimation, and deployment) can be performed in **real time** will receive higher priority, recognizing the asymmetry in real-time learning versus real-time inference;
- ❑ Proposals submitted to this program should seek to demonstrate radical improvement in the **metrics of performance**, e.g., size, weight, power, latency and energy efficiency;
- ❑ **Approximate algorithms** for efficient implementation, e.g., low-precision gradient computation and sparsely-connected neuronal nodes, are within scope;
- ❑ Approaches to **self-assessing** systems are within scope;
- ❑ **Distributed ML** algorithms and hardware for real-time performance are within scope;
- ❑ Efficient and novel utilization of data and memory paths, e.g., in- or **near-memory** computations, are within scope;
- ❑ The program is also interested in **analog/mixed-signal** architectures.



# NSF Solicitation Requirements



# Award Size and Information (NSF-RTML)

- ❑ Anticipated NSF-funding amount: \$10,000,000
- ❑ Award size:
  - **Small** Awards: up to \$500,000 for 3 years;
  - **Large** Awards: up to \$1,500,000 for 3 years.
- ❑ Estimated number of awards: 8 to 12
- ❑ Approximately \$1M of program funds reserved for “***partnership supplements***”
- ❑ Anticipated type of award: Continuing Grant
- ❑ Estimated program budget, number of awards and average award size/duration are subject to the availability of funds.



# Additional Budgetary Information

- ❑ Proposals should budget for up to two project personnel to attend **four** joint NSF-DARPA workshops over the duration of the NSF project (36 months), in the Washington DC area.
- ❑ Inclusion of voluntary committed **cost sharing** is **prohibited** for NSF proposals.



# Organization Eligibility and Limit (NSF-RTML)

- ❑ There are no restrictions or limits on the number of proposals per organization.
- ❑ U.S. *academic institutions* which perform research and with degree-granting education programs in disciplines normally supported by NSF are eligible to be the lead organization.
- ❑ *Academic institutions* are accredited two- and four-year Institutions of Higher Education having a campus in the US, acting on behalf of their faculty.
- ❑ ***Involvement of an international branch of an US institution (including subawards/consultants), must justify their involvement.***



# NSF-RTML: PI Eligibility/Limit

- ❑ Limit on Number of Proposals per PI or Co-PI: 2
  - An individual can participate as PI, co-PI, Senior Personnel, or Consultant on no more than two proposals submitted in response to this solicitation.
- ❑ The **first two** proposals received will be accepted and the remainder will be *returned without review*.
- ❑ Additionally, proposals submitted in response to this solicitation **may not duplicate** or be substantially similar to other proposals concurrently under consideration by **DARPA** (similar proposals will be *returned without review*).
- ❑ There are no restrictions on an institution from submitting to both the DARPA-RTML program and NSF-RTML program.





# NSF-RTML: PI Eligibility/Limit (cont'd)

## ❑ PI Eligibility:

Principal Investigators (PI) must be at the faculty level as determined by the submitting organization.

- ❑ DARPA Phase-I performers who do not move on to DARPA Phase-II will be eligible for NSF funding.
  - Such PIs will need to partner with an existing NSF RTML awardee on a *Large project* for collaboration through ‘*partnership supplements*’.
- ❑ DARPA teams can include researchers from NSF RTML awardees as part of their DARPA Phase 2 effort funded through ‘*partnership supplements*’.



# NSF-RTML REVIEW CRITERIA

## **Generic NSF review criteria will apply**

- ❑ National Science Board approved Merit Review Criteria
  - **Intellectual Merit**
  - **Broader Impacts**
  
- ❑ NSF Staff will give careful consideration to the following:
  - Integration of Research and Education
  - Integrating Diversity into NSF Programs, Projects and Activities



# NSF-RTML Solicitation Specific Review Criteria

The following **additional** review criteria will be used for **all** NSF-RTML proposals; all proposals should address these carefully:

- ❑ Synergy in machine learning, software, algorithm, and hardware **co-design** to meet the real-time machine learning goals of this program.

For **Large proposals**, the following **additional** review criteria will also be applied:

- ❑ strength of the **Project Management and Collaboration Plan** in the Project Description.
- ❑ strength of the **Evaluation/Experimentation plan** (e.g., in FPGA/ASIC) in the Project Description.



# Solicitation timelines

## RTML (NSF 19-566)

- ❑ **March 8, 2019**      **RTML (NSF 19-566) program announcement**
- ❑ **April 3, 2019**      **Information Webcast**
- ❑ **June 6, 2019**      **Proposals Submission Deadline**
- ❑ **Proposal review July 2019**
- ❑ NSF awards are expected to be made, pending availability of funds, **by September/October 2019**.
- ❑ A Grantee Meeting is planned for late **Fall 2019** (applications must include travel costs in proposal budget).



# Questions and Answers



# Q/A: Questions received so far ...

## Question [NSF silicon compiler]

The DARPA Phase 1 objective is a RTML hardware silicon compiler, and the outcome will be made available by DARPA to the NSF awardees as an option to evaluate their proposed new RTML approaches. In the meantime, new techniques and results produced by NSF awardees during the first 18 months will be made available to DARPA project teams for them to implement in their Phase 2 efforts to explore novel ML architectures and circuits that will enable RTML.

Does this mean that NSF RTML projects cannot include a silicon compiler as this will be part of the DARPA RTML focus? Or no such restriction exists?



## Q and A (cont'd)

### Question [FPGA]

We work in optimizing and hardware software codesign for neural models on FPGAs, with the intent of real-time performance. I noticed the following: "Proposers should be aware that routine implementations of existing AI/ML algorithms in standard hardware are not within scope of this program."

Does it mean (standard hardware) FPGAs are not relevant for this program?



# Q and A (cont'd)

Question: **[continuing grant]**

The call mentions this is a continuing grant and not a standard grant. I wanted to make sure that this information is accurate. (The NSF guidelines state that the continuation of the grant is dependent on results.)





## Q and A (cont'd)

### Question [Industry/GOALI]

I am planning to submit a LARGE RTML proposal to NSF in collaboration with a company. The project aims at developing RTML algorithms for real time control of utility scale wind farms. The company in question has terabytes of data on large wind farms, and they are essential to succeed in project goals.

Is it okay to have an industrial partner, and whether having them as subcontractor is okay, in which case, they will receive funding through a subaward (what if it is a GOALI proposal).



# Q and A (cont'd)

## Question **[EDA techniques]**

Will EDA and modeling techniques specialized for machine learning chip design be in the scope of this program?



# Q and A (cont'd)

Question: **[applications]**

Can applications of algorithms and hardware developed in the project be funded? Specifically, UAV applications, but where UAV infrastructure are supported by other funds.



# Key website URLs

**NSF-RTML webinar:**

[https://www.nsf.gov/events/event\\_summ.jsp?cntn\\_id=298083&org=CISE](https://www.nsf.gov/events/event_summ.jsp?cntn_id=298083&org=CISE)

**NSF-RTML website:**

<https://www.nsf.gov/pubs/2019/nsf19566/nsf19566.htm?org=NSF>

**DARPA-RTML website:**

[https://www.fbo.gov/index?s=opportunity&mode=form&id=29e4d24ce31d2bf276a2162fae3d11cd&tab=core&\\_cview=0](https://www.fbo.gov/index?s=opportunity&mode=form&id=29e4d24ce31d2bf276a2162fae3d11cd&tab=core&_cview=0)



***Thank you***

